## REMARKS

Reconsideration of the application in view of the above amendments and the following remarks is requested. Claims 1-4, 7-8, 10, 12, 16-19, and 21-30 are in this application. Claims 5-6, 9, 11, 13-15, and 20 have been cancelled. Claims 1-4, 7-8, 10, 12, and 16-19 have been amended. Claims 21-30 have been added to alternately claim the present invention. In addition to the amendments discussed below, the claims have also been amended to alternately claim the present invention. Further, the Summary of the Invention has been amended.

The Examiner rejected claims 1-3, 16, and 17 under 35 U.S.C. §102(b) as being anticipated by Larson et al. (U.S. Patent No. 5,481,680).

Claim 1 recites:

> "A method of adding grant information to a memory that stores information about a series of arbitration periods, the method comprising:
> "assigning a number of first addresses to a group of devices such that two or more consecutive first addresses are assigned to each device and no two devices have the same first addresses, the number of first addresses representing a corresponding number of arbitration periods such that each first address represents one arbitration period, each first address having a sequence of bits; and
> "forming a number of second addresses from the number of the first addresses such that each first address has a corresponding second address and each second address has a corresponding device by rearranging the sequence of bits in a plurality of the number of first addresses, each second address representing one arbitration period."

With respect to Larson, the list of consecutive memory addresses shown in FIG. 7 under the heading ADDRESS can not be read to be the first addresses required by claim 21 because claim 21 requires that two or more consecutive first addresses be assigned to each device. FIG. 7 of Larson, however, fails to show that

two or more consecutive memory addresses have been assigned to any device (CPU 14, DMA 16, DMA 18, or DMA 20).

For example, memory address 0001 has been assigned to a first device (CPU 14, DMA 16, DMA 18, or DMA 20) so that when address 0001 is received, the memory outputs grant G0 to the first device. In addition, the next memory address 0010 has been assigned to a second device (CPU 14, DMA 16, DMA 18, or DMA 20) so that when address 0010 is received, the memory outputs grant G1 to the second device. As a result, the consecutive memory addresses 0001 and 0010 are not assigned to the same device, but instead are assigned to two different devices which respond to grants G0 and G1.

Thus, since the Larson reference fails to teach or suggest that two or more consecutive memory addresses are assigned to each device, claim 1 is not anticipated by the Larson reference. In addition, since claims 2-4, 7-8, 10, and 12 depend either directly or indirectly from claim 1, claims 2-4, 7-8, 10, and 12 are not anticipated by the Larson reference for the same reasons as claim 1.

Claim 16 recites:

> "A communications circuit comprising:
> "a transmit circuit that transmits information onto a bus;
> "a receive circuit that receives information from the bus;
> "a memory that stores information on a series of arbitration periods; and
> "a logic circuit connected to the transmit circuit, the receive circuit, and the memory, if grant information for a group of devices is to be added to the memory, the logic circuit assigns a number of first addresses to the group of devices such that two or more consecutive first addresses are assigned to each device and no two devices have the same first addresses, the number of first addresses representing a corresponding number of arbitration periods such that each first address represents one arbitration period, each first address having a sequence of bits."

As noted above, the Larson reference fails to teach or suggest that two or more consecutive memory addresses are assigned to each device. Thus, claim 16 is not anticipated by the Larson reference. In addition, since claims 17-19 depend either directly or indirectly from claim 16, claims 17-19 are not anticipated by the Larson reference for the same reasons as claim 16.

New claim 21 recites:

> "A method of adding grant information to a memory that stores information about a series of arbitration periods, the method comprising:
> "assigning a number of first addresses to a device, the number of first addresses representing a corresponding number of arbitration periods such that each first address represents one arbitration period, each first address having a sequence of bits; and
> "forming a number of second addresses from the number of the first addresses such that each first address has a corresponding second address by rearranging the sequence of bits in a plurality of the number of first addresses, the first addresses and second addresses having an equal number of bits, each second address representing one arbitration period."

With respect to Larson, the rows of memory addresses and the corresponding rows of grant bits G0-G3 shown in FIG. 7 of Larson can not be read to be the first and second addresses, respectively, that are required by claim 21 because Larson fails to teach or suggest that the memory address in a row and the grant bits G0-G3 in a row have the same number of bits.

The Larson reference teaches that each memory address is defined by the contents of history register 50 which, as shown in FIG. 5, is 20 bits long. (See also column 3, lines 11-14 of Larson.) The list of consecutive memory addresses shown in FIG. 7 under the heading ADDRESS assumes that the H0-H3 bits of history register 50 are zero.

In the example discussed by Larson, history register 50 originally holds the memory address value 0000 0000 0000 0000 XXXX at the beginning of a first cycle. (See FIG. 6.) When the request bits 1001 are received during the first cycle, the

memory address value held by history register 50 is updated to 0000 0000 0000 0000 1001. This address is then used to access the memory which, as shown in FIG. 7, produces the output value of 0001.

The output value of 0001 is then placed into the H0 field so that, at the beginning of a second cycle before the next request bits have been received, history register 50 holds the memory address value of 0000 0000 0000 0001 XXXX. (See FIG. 8 and column 5, lines 54-59 of Larson.) When the request bits 1001 are again received during the second cycle, the memory address value held by history register 50 is updated to 0000 0000 0000 0001 1001.

This address is then used to access the memory (which is not shown in FIG. 7 because the H0-H3 values are assumed to be zero in FIG. 7) to produce the output value of 1000. The output value of 1000 is then placed in the H0 field, while the previous output value of 0001 is placed in the H1 field. At this point, history register 50 holds the memory address value of 0000 0000 0001 1000 XXXX. (See FIG. 9 and column 6, lines 3-5 of Larson.)

Thus, Larson teaches that the number of bits in each memory address is 20. On the other hand, FIG. 7 of Larson teaches that the number of grant bits G0-G3 in each row is four. As a result, the rows of memory addresses and the corresponding rows of grant bits G0-G3 shown in FIG. 7 of Larson can not be read to be the first and second addresses, respectively, that are required by claim 21 because the number of bits (20) in each row of memory addresses is not equal to the number of bits (four) in each row of grant bits.

Therefore, since the number of memory address bits in each row is not equal to the number of grant bits in each row, claim 21 is not anticipated by the Larson reference. In addition, since claims 22-25 depend either directly or indirectly from claim 21, claims 22-25 are not anticipated by Larson for the same reasons as claim 21.

New claim 26 recites:

> "A method of adding grant information to a memory that stores information on a series of arbitration periods, the method comprising:
> "assigning a number of first addresses to a device, the number of first addresses representing a corresponding number of arbitration periods such that each first address represents one arbitration period, no two first addresses being identical, each first address having a sequence of bits; and
> "forming a number of second addresses from the number of the first addresses such that each first address has a corresponding second address by rearranging the sequence of bits in a plurality of the number of first addresses, each second address representing one arbitration period, no two second addresses being identical."

With respect to Larson, the rows of grant bits G0-G3 shown in FIG. 7 can not be read to be the number of second addresses required by claim 26 because claim 26 requires that no two second addresses can be identical. As shown in FIG. 7, Larson teaches that the contents of grant bit rows 2, 4, 6, 8, 10, 12, 14, and 16 are identical, each having the value of 0001.

Therefore, since the rows of grant bits G0-G3 shown in FIG. 7 can not be read to be the number of second addresses required by claim 26 because a number of the rows of grant bits G0-G3 are identical, claim 26 is not anticipated by the Larson reference. In addition, since claims 27-30 depend either directly or indirectly from claim 26, claims 27-30 are not anticipated by Larson for the same reasons as claim 26.

The Examiner objected to claims 4, 11, 14-15, and 18-19, but indicated that these claims would be allowable if rewritten in independent form to include all of the limitations of the base claim and any intervening claims. In view of the above amendments and discussion, claims4, 11, 14-15, and 18-19 have not been amended to be in independent form.

Thus, for the foregoing reasons, it is submitted that all of the claims are in a condition for allowance. Therefore, the Examiner's early re-examination and reconsideration are respectively requested.

Respectfully submitted,

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